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10/765,581	01/27/2004	Brian Johnson	200210236-1	1503

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
05/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
mkraft@hp.com
ipa.mail@hp.com

Office Action Summary	Application No.	Applicant(s)	
	10/765,581	JOHNSON ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 03/04/2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Robert W. Beausoliel, Jr./

Supervisory Patent Examiner, Art Unit 2113.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1,7,15,17-21,23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Mates (USPN 6564347B1). As per claim 1, Mates discloses a first device arranged on a circuit board in column 3, lines 7-18; and a programmable capture device arranged on said circuit board, wherein at least one input pin of said programmable capture device is communicatively coupled to at least one externally-accessible signal pin of said first device such that said programmable capture device captures at least one signal from said first device during testing of said first device in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

4. As per claim 7, Mates discloses wherein said first device comprises an Application-Specific Integrated Circuit (ASIC) in column 4, lines 11-12. A microprocessor is an ASIC.

5. As per claim 15, Mates discloses triggering testing of a first device arranged on a circuit board in column 3, lines 7-18; and capturing data from an externally-accessible signal pin of said first device during said testing by a separate field-programmable data capture device also arranged on said circuit board in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

6. As per claim 17, Mates discloses programming the field-programmable data capture device to capture desired data from the first device in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

7. As per claim 18, Mates discloses wherein said programming comprises: programming the field-programmable data capture device while said field-programmable data capture device is arranged on said circuit board in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

8. As per claim 19, Mates discloses communicatively coupling a control system to said field-programmable data capture device arranged on said circuit board for performing the programming in column 2, lines 50-67; column 5, lines 46-58.

9. As per claim 20, Mates discloses wherein the programming comprises selecting at least one signal pin of said first device from which data is to be captured by said field-programmable data capture device in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

10. As per claim 21, Mates discloses a first means for performing an operation, wherein said first means is arranged on a circuit board in column 3, lines 7-18; and a means external to said first means, arranged on said circuit board, for capturing signals from an externally-accessible pin of said first means during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

11. As per claim 23, Mates discloses means, arranged external to said circuit board, for programming the capturing means in column 2, lines 50-67; column 5, lines 46-58.

12. As per claim 24, Mates discloses wherein the programming comprises selecting at least one signal pin of the first means from which signals are to be captured by the

capturing means in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58.

13. As per claim 25, Mates discloses wherein the capturing means comprises a plurality of input pins that are each communicatively coupled to a different signal pin of the first means, and wherein the capturing means is programmable to select at least one of said input pins that is to have its received signals output at an output pin of the capturing means in column 2, lines 26-29; in column 3, lines 15-24; in column 4, lines 45-49; in column 5, lines 46-58. The test vectors are on the pins of the components to be tested.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2,3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mates in view of Zeng et al. (USPN 6243272B1).

16. As per claim 2, Mates fails to explicitly state wherein said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side.

Zeng et al. discloses this limitation in column 3, lines 33-46.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first device is arranged on a first side of said

circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side. A person of ordinary skill in the art would have been motivated to have said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side because the size of the circuit board is decreased by having chips on both sides.

17. As per claim 3, Mates fails to explicitly state wherein said programmable capture device comprises pins having an arrangement corresponding to an arrangement of pins of the first device.

Zeng et al. discloses this limitation in column 7, lines 1-3.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said programmable capture device comprise pins having an arrangement corresponding to an arrangement of pins of the first device. A person of ordinary skill in the art would have been motivated to have said programmable capture device comprise pins having an arrangement corresponding to an arrangement of pins of the first device because the pin arrangements can be representative of identical components.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mates in view of Zeng et al. (USPN 6243272B1) in further view of Clabes et al. (US Publication Number 20030074645A1).

As per claim 4, Mates and Zeng et al. fail to explicitly state wherein said first device comprises at least one-thousand signal pins.

Clabes discloses this limitation on page 1, paragraph 0008.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first device comprise at least one-thousand signal pins. A person of ordinary skill in the art would have been motivated to have said first device comprise at least one-thousand signal pins because the pins represent the arrangement of a circuit board.

19. Claims 5,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mates in view of Clabes et al. (US Publication Number 20030074645A1).

Mates fails to explicitly state wherein said programmable capture device has a density of input pins on order of signal pins of said first device.

Clabes discloses this limitation on page 1, paragraph 0008.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said programmable capture device has a density of input pins on order of signal pins of said first device. A person of ordinary skill in the art would have been motivated to have said programmable capture device has a density of input pins on order of signal pins of said first device because the pins represent the arrangement of a circuit board.

20. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mates in view of Clabes et al. (US Publication Number 20030074645A1) in further view of Zeng et al.

21. As per claim 6, Mates fails to explicitly state wherein said first device comprises at least one-thousand signal pins.

Clabes discloses this limitation on page 1, paragraph 0008.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first device comprise at least one-thousand signal pins. A person of ordinary skill in the art would have been motivated to have said first device comprise at least one-thousand signal pins because the pins represent the arrangement of a circuit board.

22. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mates in view of Bailis et al. (USPN 6243272B1).

23. As per claim 8, Mates fails to explicitly state wherein said programmable capture device comprises a Field Programmable Gate Array (FPGA).

Bailis et al. discloses this limitation on pages 1 and 2, paragraph 0015.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said programmable capture device comprise a Field Programmable Gate Array (FPGA). A person of ordinary skill in the art would have been motivated to have said programmable capture device comprise a Field Programmable Gate Array (FPGA) because a FPGA is capable of being programmed to perform a function.

24. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mates (USPN 6564347B1) in view of Mates (USPN 7089473B2) in further view of Dervisoglu et al. (USPN 6687865B1).

25. As per claim 9, Mates (USPN 6564347B1) fails to explicitly state programmable capture device communicatively coupled to an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board.

Mates (USPN 7089473B2) discloses this limitation in column 5, lines 18-39; column 7, lines 6-24. Mates '473 discloses a logic analyzer unit which has one portion on the same circuit board as the first device which functions as the programmable capture device and a second portion on an external probe that has the functionality of a logic analyzer that analyzes the results. The interface is the probe electrical connection points.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have programmable capture device communicatively coupled to an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board. A person of ordinary skill in the art would have been motivated to have programmable capture device communicatively coupled to an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board because the captured data can be sent to be analyzed by the logic analyzer.

Mates (6564347B1) and Mates (7089473B2) fail to explicitly state at least one output pin coupled to the interface.

Dervisoglu et al. discloses this limitation in column 1, lines 13-20.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have programmable at least one output pin coupled to

the interface. A person of ordinary skill in the art would have been motivated to have at least one output pin coupled to the interface because connections are provided so the captured data can be sent to be analyzed by the logic analyzer.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mates (USPN 6564347B1) in view of Mates (USPN 7089473B2) in view of Dervisoglu et al. (USPN 6687865B1) in further view of Josephson et al. (USPN 5530706A).

27. As per claim 10, Mates, Mates, and Dervisoglu et al. fail to explicitly state wherein said testing of said first device comprises testing said first device at its normal operating frequency.

Josephson et al. discloses this limitation in column 1, line 65 – column 2, line 2.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said testing of said first device comprises testing said first device at its normal operating frequency. A person of ordinary skill in the art would have been motivated to have said testing of said first device comprises testing said first device at its normal operating frequency because there is no compromising of the integrity of the data being captured from the device at normal operating frequency in spite of the clocking of the test circuitry, see column 1, lines 54-58.

28. Claims 11,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mates (USPN 6564347B1) in view of Mates (USPN 7089473B2) in view of Dervisoglu et al. (USPN 6687865B1) in view of Josephson et al. (USPN 5530706A) in further view of DenBeste et al. (USPN 4558422).

29. As per claim 11, Mates, Mates, Dervisoglu et al., and Josephson et al. fail to explicitly state wherein said logic analyzer has an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

DenBeste et al. discloses this limitation in column 1, lines 35-53.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer. A person of ordinary skill in the art would have been motivated to have said logic analyzer have an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer because data can be captured at different frequencies.

30. As per claim 13, Mates fails to explicitly state wherein said logic analyzer has an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

DenBeste et al. discloses this limitation in column 1, lines 35-53.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer. A person of ordinary skill in the art would have been motivated to have said logic analyzer have an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer because data can be captured at different frequencies.

31. Claims 12,14,16,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mates (USPN 6564347B1) in view of Mates (USPN 7089473B2).

32. As per claim 12, Mates (6564347B1) fails to explicitly state wherein the programmable capture device parallelizes the captured signals.

Mates (7089473B2) discloses this limitation in column 9, lines 2-5.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have the programmable capture device parallelizes the captured signals. A person of ordinary skill in the art would have been motivated to have said logic analyzer have the programmable capture device parallelizes the captured signals because data can be sent through various signals and buses in different formats.

33. As per claim 14, Mates (6564347B1) fails to explicitly state wherein the programmable capture device serializes the captured signals.

Mates (7089473B2) discloses this limitation in column 9, lines 2-5.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have the programmable capture device serializes the captured signals. A person of ordinary skill in the art would have been motivated to have said logic analyzer have the programmable capture device serializes the captured signals because data can be sent through various signals and buses in different formats.

34. As per claim 16, Mates (6564347B1) fails to explicitly state outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board.

Mates (USPN 7089473B2) discloses this limitation in column 5, lines 18-39; column 7, lines 6-24. Mates '473 discloses a logic analyzer unit which has one portion on the same circuit board as the first device which functions as the programmable capture device and a second portion on an external probe that has the functionality of a logic analyzer that analyzes the results. The interface is the probe electrical connection points.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board. A person of ordinary skill in the art would have been motivated to

have outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board because the captured data can be sent to be analyzed by the logic analyzer.

35. As per claim 22, Mates (6564347B1) fails to explicitly state a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means.

Mates (USPN 7089473B2) discloses this limitation in column 5, lines 18-39; column 7, lines 6-24. Mates '473 discloses a logic analyzer unit which has one portion on the same circuit board as the first device which functions as the programmable capture device and a second portion on an external probe that has the functionality of a logic analyzer that analyzes the results. The interface is the probe electrical connection points.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means. A person of ordinary skill in the art would have been motivated to have a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means because the captured data can be sent to be analyzed by the logic analyzer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yolanda L Wilson/
Primary Examiner, Art Unit 2113